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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,640	05/02/2006	Toshihide Tsubata	70404.90/ma	3891

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EXAMINER	
TAYLOR, EARL N	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
07/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/595,640	TSUBATA ET AL.	
	Examiner	Art Unit	
	Earl N. Taylor	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2 May 2006 to 13 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/2/2006, 10/3/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-5 and 8, in the reply filed on 13 July 2007 is acknowledged.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statements (IDS) filed on 2 May 2006 and 3 October 2006. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (U.S. Patent 5,834,345).

Referring to Claims 1 and 2, Shimizu teaches, in Fig. 1 for example, a transistor comprising: a source electrode and a drain electrode (7 and 8); arranged in mutually opposing relation; a semiconductor film comprising at least one layer (5) disposed between the source electrode and the drain electrode (7 and 8); a gate electrode (2) disposed in adjacent relation to the semiconductor film (5); and a gate insulating film (3) disposed between the gate electrode (2) and each of the source electrode, the drain electrode, (7 and 8) and the semiconductor film (5), wherein the gate insulating film (3) does not contain a concentration of fluorine, meaning the concentration of fluorine is zero, which anticipates the range of 1 x 10^{20} atoms/cm^3 or less and the range of 1 x 10^{19} atoms/cm^3 or less (Col. 3, Lines 55 to Col. 4, Line 7).

Referring to Claim 3, Shimizu teaches all of the limitations of Claim 1, which is of a field-effect type (Col. 1, Lines 6-10).

Referring to Claim 4, Shimizu teaches all of the limitations of Claim 1, wherein the gate insulating film is an amorphous silicon nitride film (Col. 3, Lines 55-65).

Referring to Claim 5, Shimizu teaches all of the limitations of Claim 1, wherein the gate insulating film is deposited by a CVD method (Col. 3, Lines 55-65). Furthermore, The language, term, or phrase "the gate insulating film is deposited by a CVD method", is directed towards the process of depositing a film. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See

also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the claim language only requires a gate insulating film, which does not distinguish the invention from Yamazaki, who teaches the structure as claimed.

Referring to Claim 8, Shimizu teaches all of the limitations of Claim 1 wherein a liquid crystal display device comprising the transistor of claim 1 as a switching element for a pixel electrode portion (Col. 1, Lines 6-10).

Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (U.S. Patent 5,837,614).

Referring to Claims 1 and 2, Yamazaki teaches, in Fig. 2 for example, a transistor comprising: a source electrode and a drain electrode (source/drain, 212 and 213); arranged in mutually opposing relation; a semiconductor film (203) comprising at least one layer (208) disposed between the source electrode and the drain electrode (212 and 213); a gate electrode (205) disposed in adjacent relation to the

semiconductor film (203); and a gate insulating film (204) disposed between the gate electrode (205) and each of the source electrode, the drain electrode, (212 and 213) and the semiconductor film (208), wherein a concentration of fluorine contained in the gate insulating film (204) is 1 x 10^{17} atoms/cm^3 to 5 x 10^{20} atoms/cm^3, which anticipates the range of 1 x 10^{20} atoms/cm^3 or less and the range of 1 x 10^{19} atoms/cm^3 or less (Col. 2, Lines 13-18 and Col. 3, Lines 18-21).

Referring to Claim 3, Yamazaki teaches all of the limitations of Claim 1, which is of a field-effect type.

Referring to Claim 5, Yamazaki teaches all of the limitations of Claim 1, wherein the gate insulating film is deposited by a CVD method (abstract; Col. 4, Lines, 48-59). Furthermore, The language, term, or phrase "the gate insulating film is deposited by a CVD method", is directed towards the process of depositing a film. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims

or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the claim language only requires a gate insulating film, which does not distinguish the invention from Yamazaki, who teaches the structure as claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent 5,837,614) in view of Ohta et al. (Ultrathin fluorinated silicon nitride gate dielectric films formed by remote plasma enhanced chemical vapor deposition employing NH_3 and SiF_4).

Referring to Claim 4, Yamazaki teaches all of the limitations of Claim 1, wherein the gate insulating film is an amorphous silicon nitride film. However, Ohta teaches having a gate insulating film comprising fluorinated silicon nitride by CVD. Therefore it would have been obvious to one having ordinary skill in the art to provide the silicon nitride film of Ohta as the gate insulating film instead of the silicon oxide film of Yamazaki in order to increase the dielectric constant and provide a device low leakage current (abstract).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references teach amorphous silicon nitride as a gate insulating layer:

- Hong et al. (U.S. Patent 7,220,991 B2) (Col. 13, Line 21; Col. 30, Lines 9-12).
- Choi et al. (U.S. Patent 7,095,460 B2) (Col. 16, Lines 55-60).
- Inaba et al. (U.S. Patent 4,838,652) Fig. 9
- Mizutani et al. (U.S. Patent 5,812,284)

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

STEVEN LOKE
SUPERVISORY PATENT EXAMINER

Steven Loke